Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-10. (canceled)

11. (original) A method of manufacturing a semiconductor device, comprising:

forming an insulating layer on a substrate;

forming a fin structure on the insulating layer, the fin structure including a first side surface, a second side surface, and a top surface;

forming source and drain regions at ends of the fin structure;

depositing a gate material over the fin structure, the gate material surrounding the top surface and the first and second side surfaces;

etching the gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin; and

planarizing the deposited gate material proximate to the fin.

12. (original) The method of claim 11, further comprising:

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

13. (original) The method of claim 11, further comprising:

forming a dielectric layer over the top surface of the fin structure.

14. (original) The method of claim 13, wherein the planarizing includes:

polishing the gate material so that no gate material remains above the dielectric layer.

15. (original) The method of claim 11, further comprising:

growing oxide layers on the first side surface and the second side surface of the fin structure.

16-20. (canceled)

21. (new) A method of manufacturing a semiconductor device, comprising:

forming a fin on an insulating layer, the fin including side surfaces and a top surface;

depositing a gate material over the fin;

etching the gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin; and

removing the deposited gate material from over the top surface of the fin.

22. (new) The method of claim 21, further comprising:

forming source and drain regions at ends of the fin;

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

23. (new) The method of claim 21, further comprising:

forming a dielectric cap on the top surface of the fin.

24. (new) The method of claim 23, wherein the removing includes:

polishing the gate material down to the dielectric cap.

25. (new) The method of claim 21, further comprising:

growing oxide layers on the opposite sides of the fin.

26. (new) A method of manufacturing a semiconductor device, comprising:

forming a fin on an insulating layer;

forming gate dielectric layers on opposite sides of the fin;

depositing a gate material over the fin and proximate the gate dielectric layers;

etching the gate material to form a first gate electrode and a second gate electrode on the opposite sides of the fin; and

removing a portion of the deposited gate material to electrically separate the first gate electrode from the second gate electrode.

27. (new) The method of claim 21, further comprising:

forming source and drain regions at ends of the fin;

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

28. (new) The method of claim 26, further comprising:

forming a dielectric cap on a top surface of the fin.

29. (new) The method of claim 28, wherein the removing includes:

polishing the gate material down to the dielectric cap.

30. (new) The method of claim 26, wherein a thickness of each of the gate dielectric layers is between about 10 Å and about 50 Å.

31. (new) The method of claim 26, wherein a thickness of the gate material is between about 300 Å and about 1500 Å.